AND8368/D

AMIS−4168x Fault Tolerant CAN Transceiver

Start−up Behavior

Prepared by:
ON Semiconductor

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

Introduction

This document discusses the start−up behavior of AMIS−41682.

Schematic Diagram

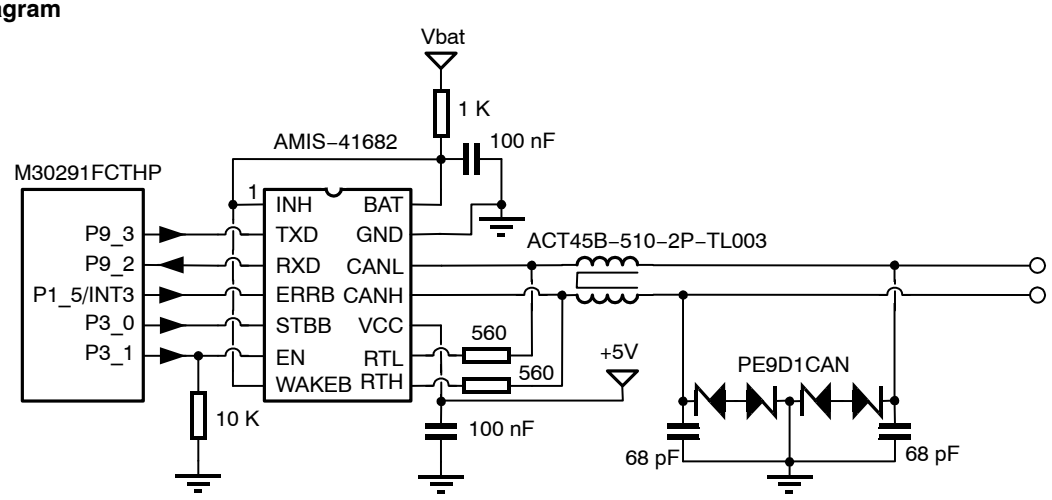


Figure 1. Application Diagram CANLSFT

In Figure 1 the customer schematic diagram of the application is illustrated. The microcontroller is supplied from the same 5 V regulator. An internal POR keeps all I/O's in tri−state (HiZ) during 32 ms. See also Figure 2.

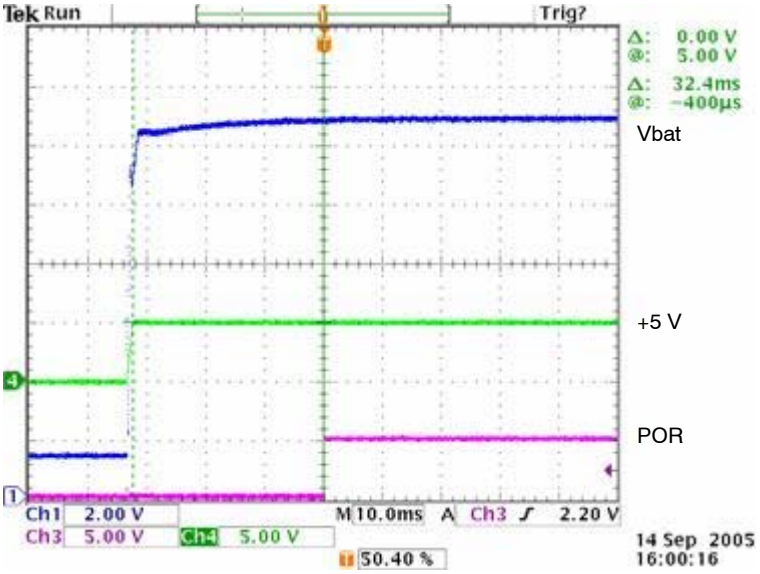
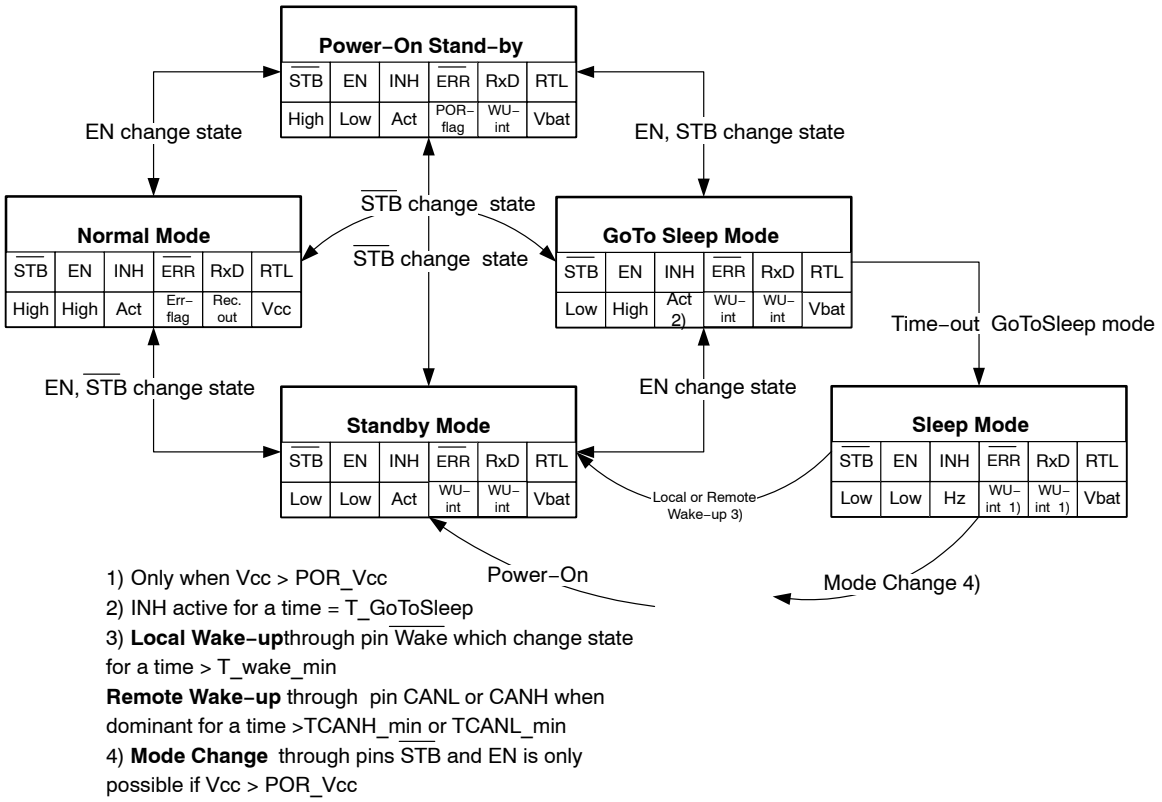


Figure 2. POR of the Microcontroller

Customer Observation

After start−up one would expect RXD = 1. This is based on the state diagram as illustrated in Figure 3.



1) Only when Vcc > POR_Vcc
2) INH active for a time = T_GoToSleep
3) **Local Wake−up**through pin $\overline{\text{Wake}}$ which change state for a time > T_wake_min
Remote Wake−up through pin CANL or CANH when dominant for a time >TCANH_min or TCANL_min
4) **Mode Change** through pins $\overline{\text{STB}}$ and EN is only possible if Vcc > POR_Vcc

Figure 3. State Diagram Low Power Modes

Because both EN = 0 and STBB = 0 the IC will enter stand−by mode. The RXD pin will output the WU detector. Because WAKEB is connected to Vbat (see Figure 1) and because there is no dominant state on the CAN−bus (see Figure 4) RXD is expected to stay “1”.

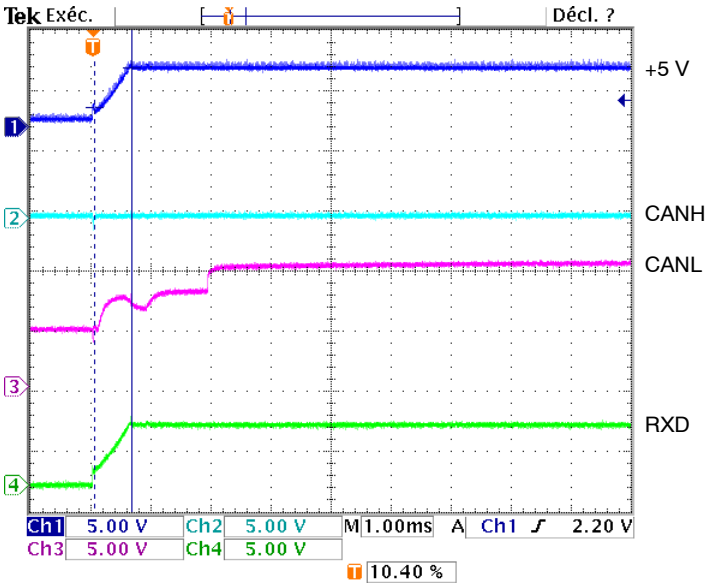


Figure 4. Expected Start−up Behavior

This expected behavior is only seen from time to time. In most cases the RXD stays low. This is illustrated in Figure 5. It looks like RXD is starting up correctly, but turns to zero after about hundred microseconds. Figure 6 is a zoom in.

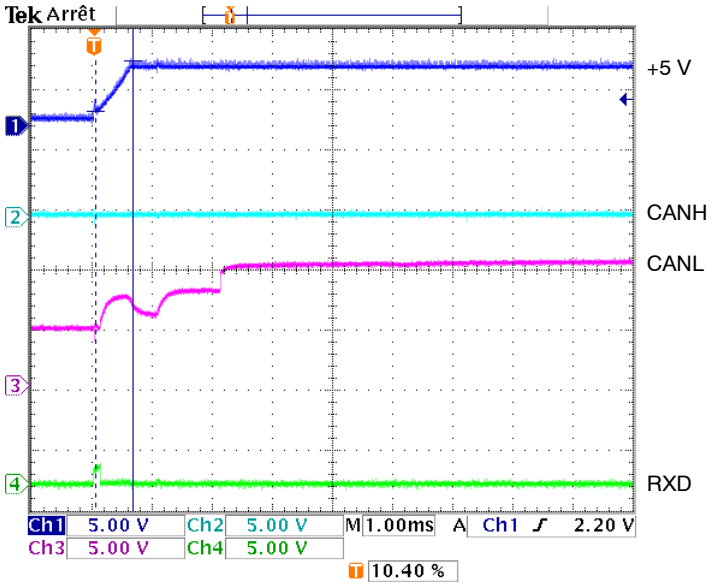


Figure 5. Observed Start−up Behavior

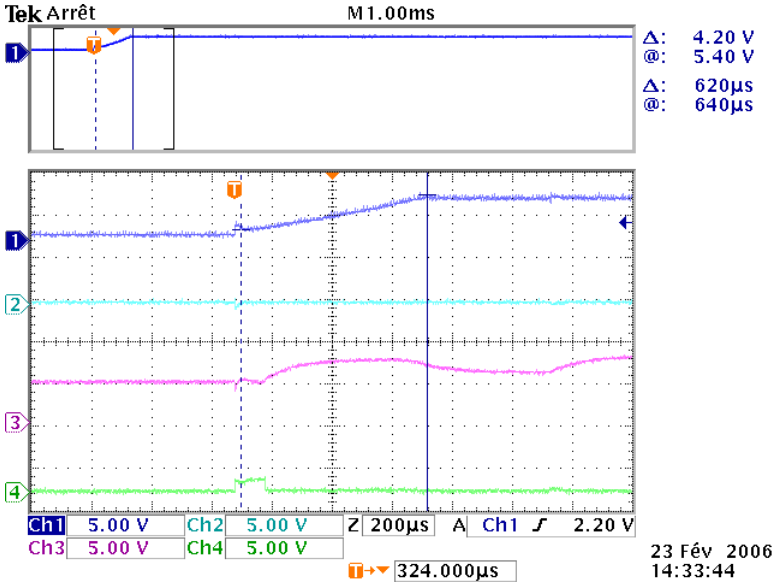


Figure 6. Zoom In of Observed Start−up Behavior

Observations

Figure 7 illustrates the used measurement set−up. Different switches allow isolation of the CAN−bus; to put EN and STBB to ground, VCC or floating; to create a wake−up and to switch on/off the power. A separate 5 V regulator ensures that the +5 V is powered up synchronous to Vbat. The left transceiver is the device under test (DUT). The transceiver on the right is used as buskeeper to put the CAN−bus in a permanent dominant state. This IC is permanent supplied.

Used equipment:

- Oscilloscope type: Agillent Infiniium 600 MHz, 4 GSa/s
- Power supply: Thurlby Thandar Instruments PL320QMD

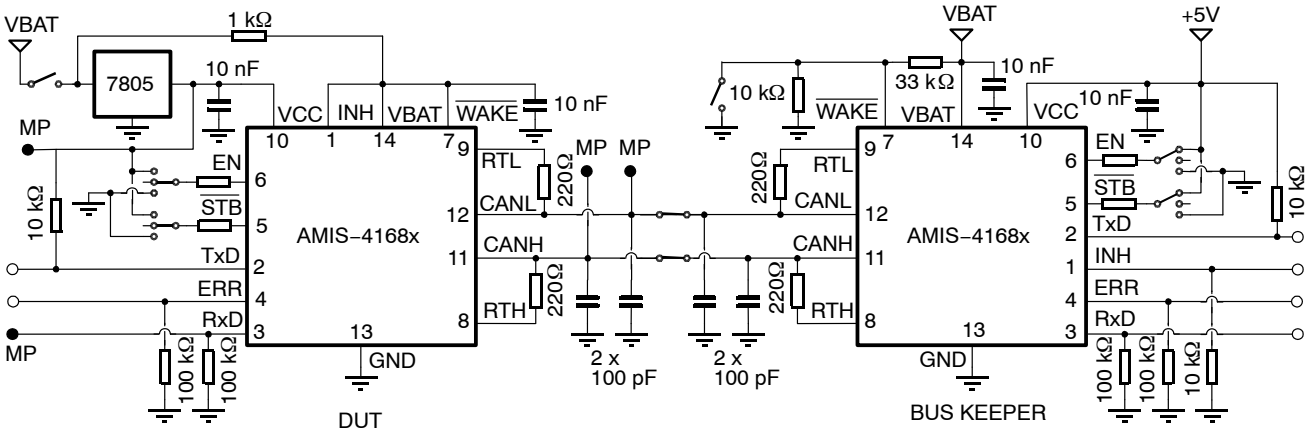


Figure 7. Measurement Set−up

The oscilloscope plots are showing the signals measured on the different measurement points (MP).

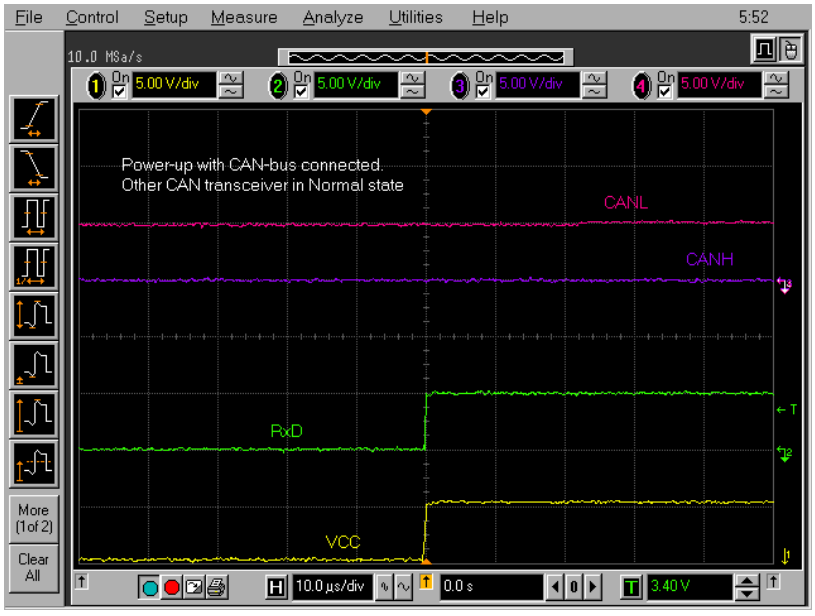


Figure 8. Power− up using set−up in Figure 7. The CAN−bus is in a permanent recessive state (CANL = VCC). RxD becomes high after power−up of VCC.

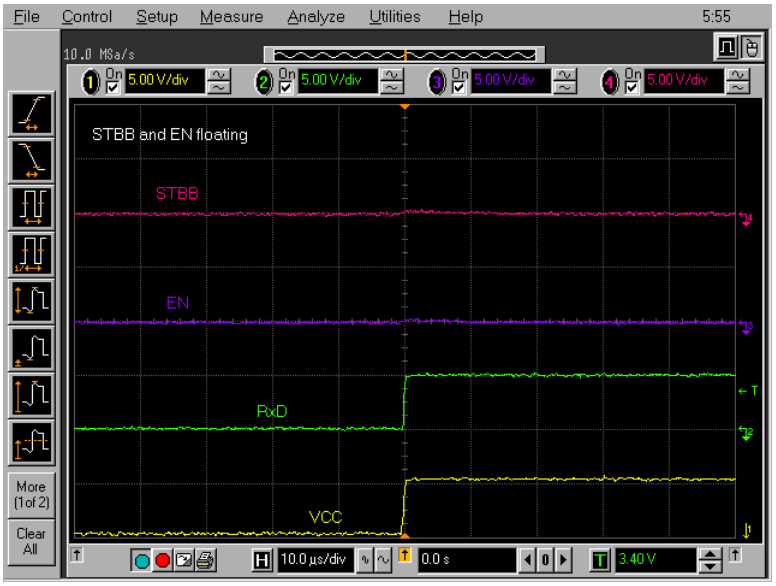


Figure 9. Power−up using set−up in Figure 7. Both STBB as EN are kept floating. The internal pull down resistors are keeping both levels low, also, during the rising edge of VCC. RxD becomes high after power−up of VCC.

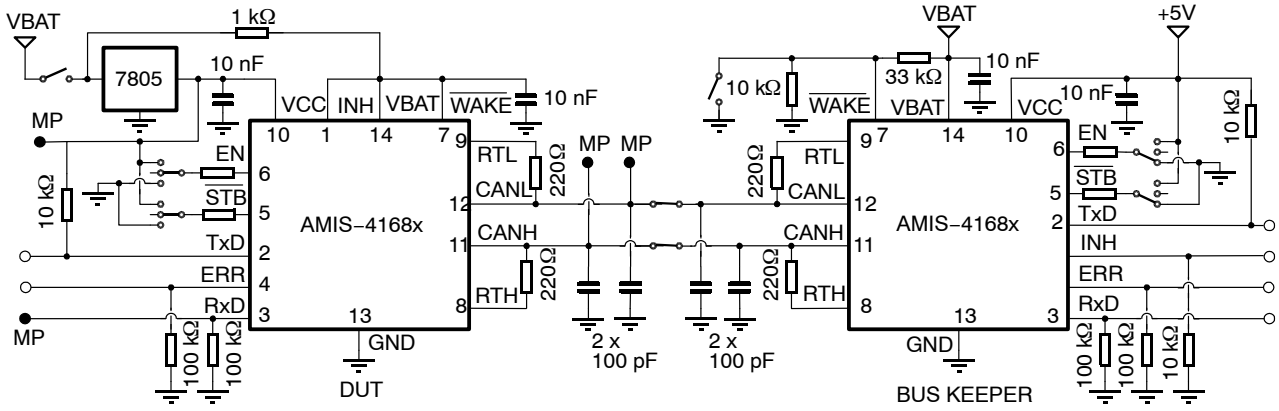


Figure 10. Measurement Set−up: Buskeeper in Stand−by State: EN = STBB = 0

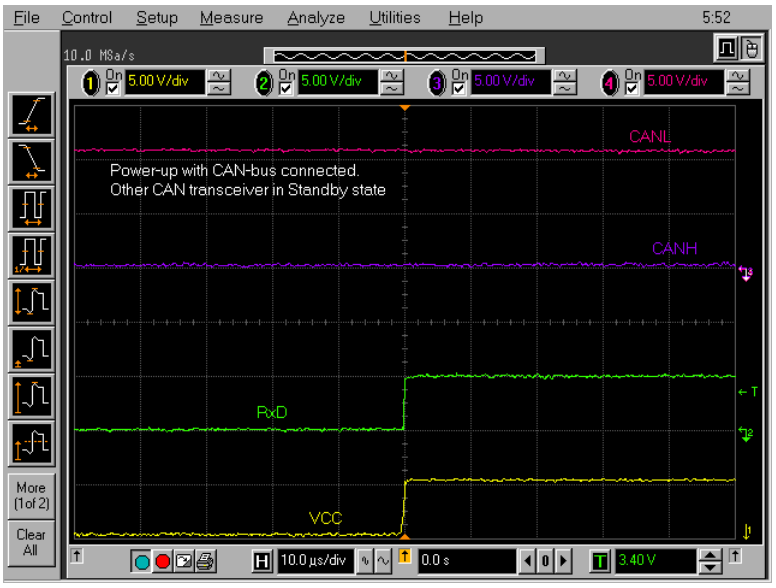


Figure 11. Power−up using set−up in Figure 10. The CAN−bus is in a permanent recessing state (CANL = VBAT) with the buskeeper in stand−by state. RxD becomes high after power−up of VCC.

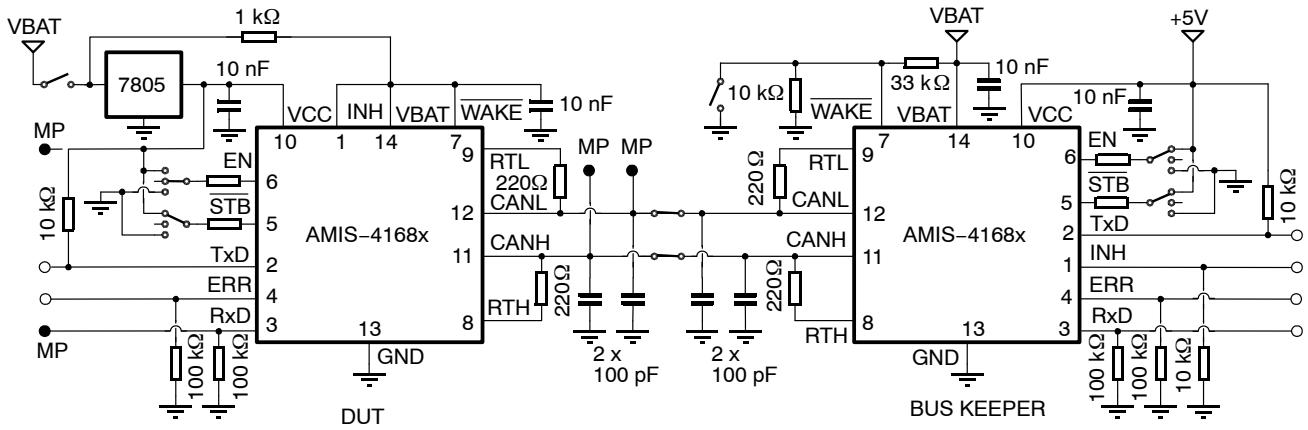


Figure 12. Measurement set−up: buskeeper in normal mode: EN = STBB = 1. For DUT EN = floating (internally pulled down) and STBB = 1.

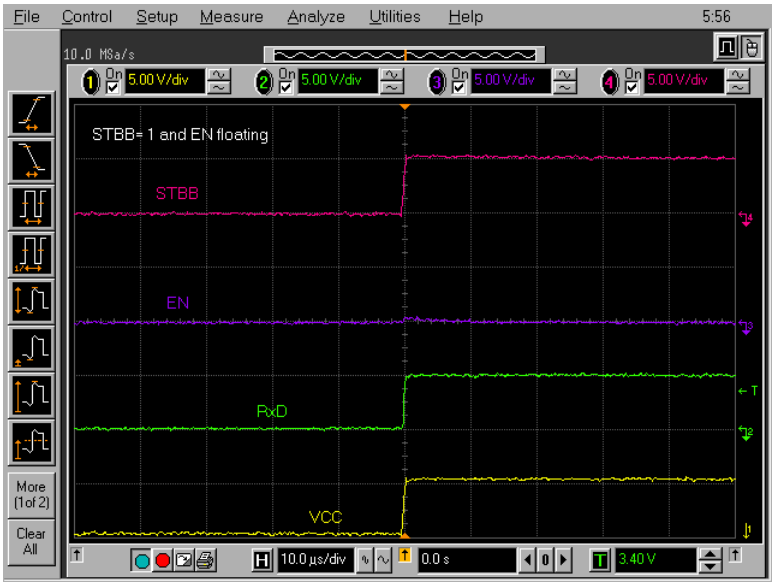


Figure 13. Power−up using set−up in Figure 12. The CAN−bus is in a permanent recessive state (CANL = VCC) with the buskeeper in normal mode. STBB = 1 and EN is floating (pulled down internally). RxD becomes high after power−up of VCC.

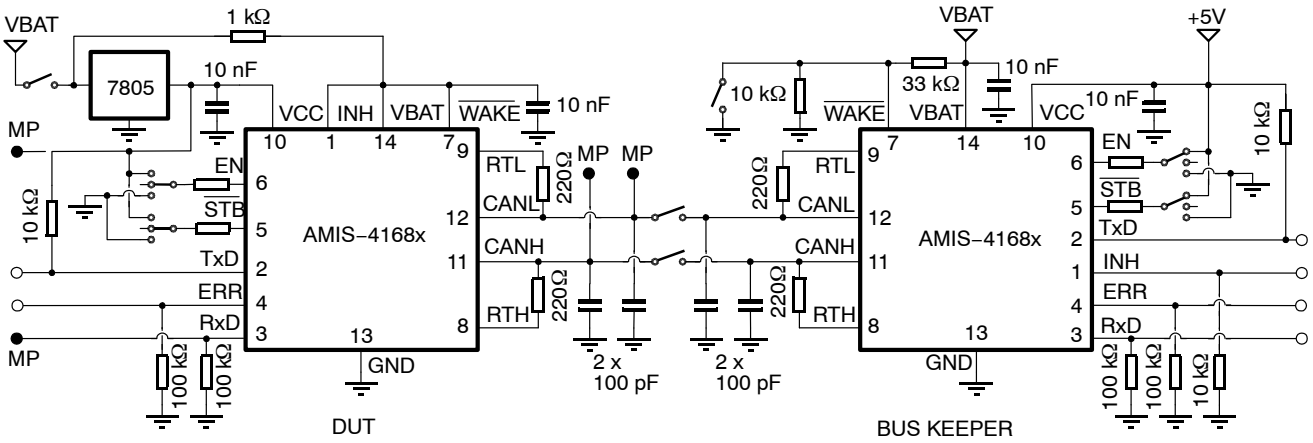


Figure 14. Measurement set−up: CAN−bus is open. Both EN = STBB = 0 (internally pulled down).

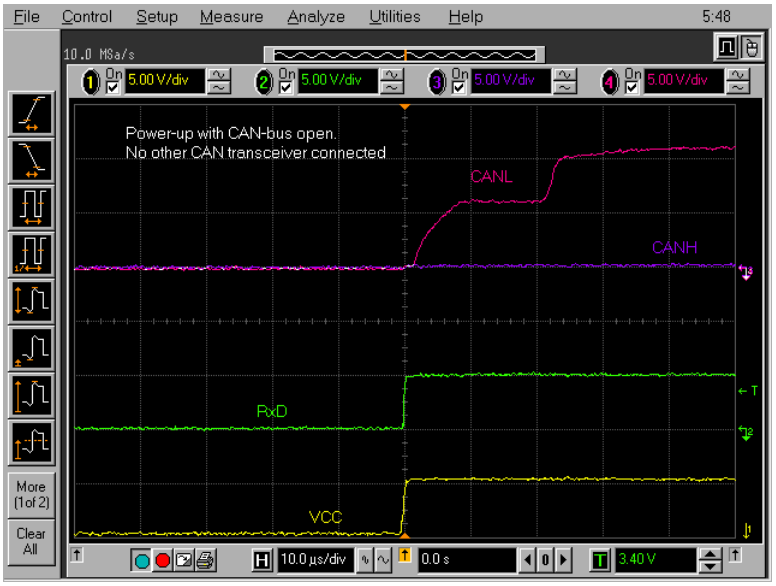


Figure 15. Power−up using set−up in Figure 14. The CAN−bus is open. RxD becomes high after power−up of VCC.

Proposed Start−up Procedure

Under very specific conditions (the individual power−on rise time and delay between Vcc and Vbat) the chance exists that RxD stays 0 after start−up. This very specific condition is illustrated in Figure 16.

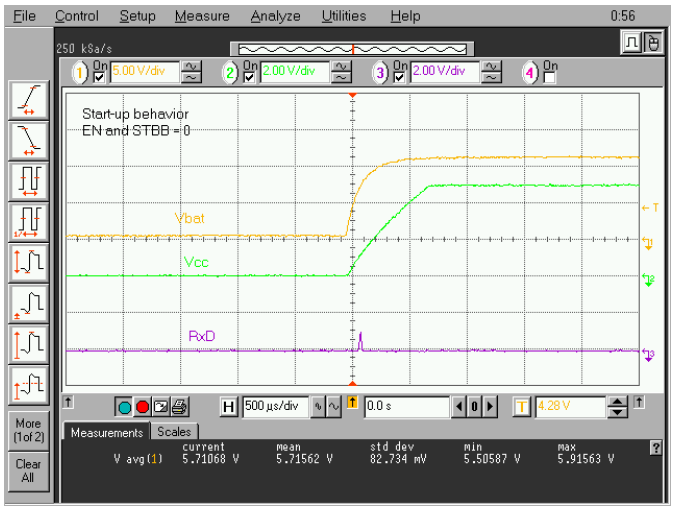


Figure 16. RxD stays low under specific conditions for Vcc and Vbat rise times and delay.

By changing the power−on rise times and/or changing the delay between Vbat and Vcc, it is possible to increase the probability to have RxD = 1, but this probability can never be guaranteed to be one.

For that reason ON Semiconductor advises to perform a short initialization using the digital input pins STBB and EN as described in Table 1. See also Figure 3.

Table 1. Initialization Sequence

State	STBB	EN	Duration
Start−up	X	X	−
Power−on stand−by	1	0	6.4 µs
Normal mode	1	1	5.8 µs
GoTo sleep mode	0	1	Time out GoTo sleep
Sleep mode	0	1	

This sequence guarantees 100 percent that RxD = 1. Measurements were done using the test set−up illustrated in Figure 17. When the power is switched on the POR circuit is creating a “start−pulse” to the microcontroller triggering the sequence on the STBB and EN pins:

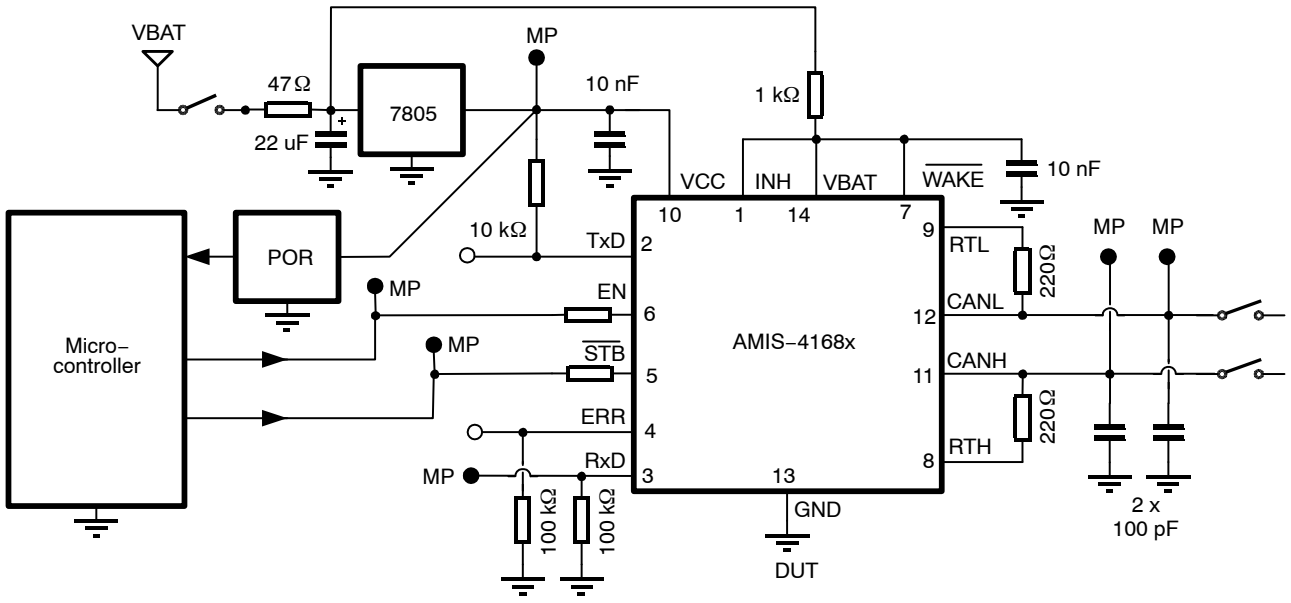


Figure 17. Measurement Set−up to Check the Initialization

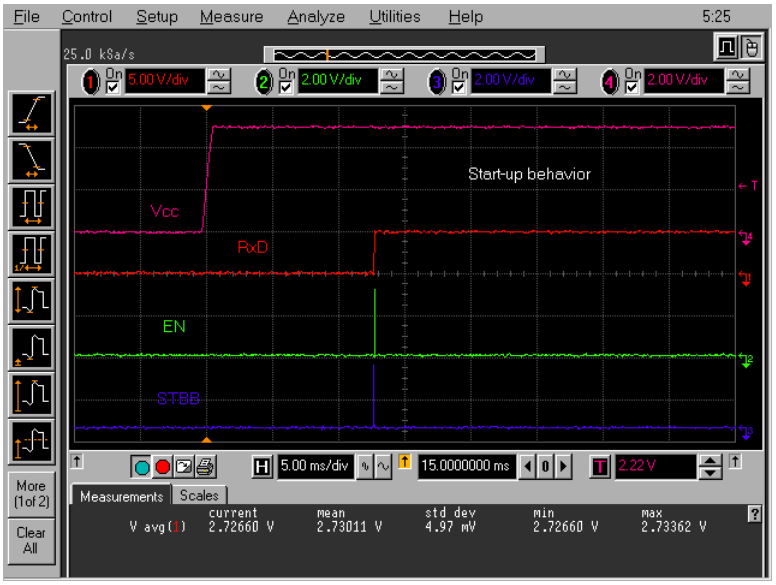


Figure 18. Start−up Behavior using the Proposed Sequence from Table 1

In Figure 18 the behavior is shown. Vcc comes up with a rise−time of about 600 μs. After a POR delay of 13 ms STBB and EN are toggled. In return RxD switches high.

Figure 19 shows the influence on the CANL line.

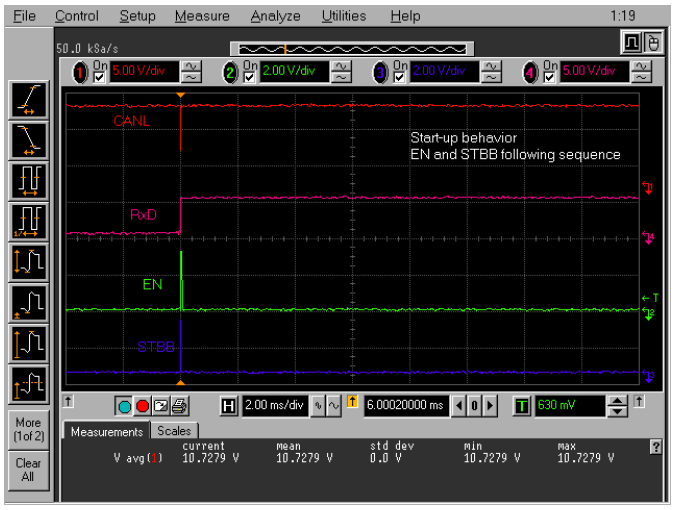


Figure 19. Start−up behavior using the proposed sequence from Table 1. Influence on the CANL line.

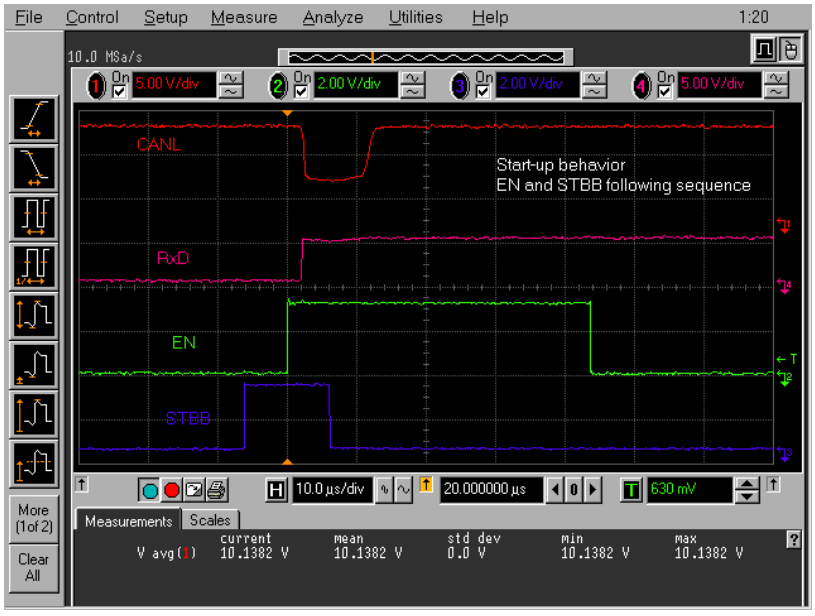


Figure 20. Zoomed in View of Figure 19

Because we enter the normal mode for 5.8 µs, CANL is pulled−up via RTL to Vcc for a very short while: 9.6 µs. This is about 1.2 Tbit (for baudrate = 125 kbit/s).

This short change in termination voltage level does not influence the communication on the bus because it stays a clean recessive level. (The CANL level is under all conditions above the maximum receiver threshold level = 3.4 V).

To evaluate this, the buskeeper is (re)connected to the CAN bus. (See Figures 10 and 12). With the buskeeper in stand−by mode, RxD_buskeeper is monitored. As shown in Figure 21 no effect is observed. The CAN bus stays in recessive state and no wake−up is possible.

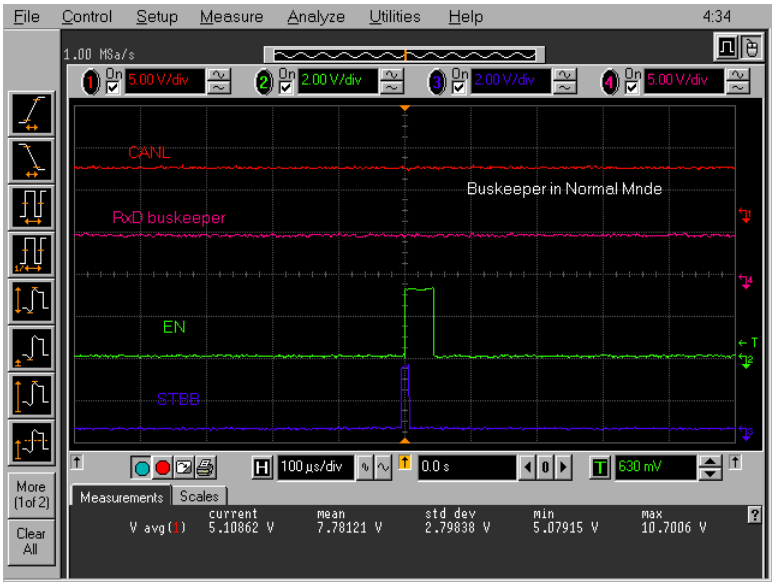


Figure 21. Buskeeper in stand−by mode. CANL termination switched from Vbat to Vcc for a short while (1.2 Tbits). No influence seen on RxD_buskeeper.

With the buskeeper in normal mode the bus will be terminated to Vcc and ground (respectively for CANL and CANH). As a result the short “change” in bus termination voltage will even not be observable. Also in this case RxD_buskeeper is monitored. As shown in Figure 22 no effect is observed. The CAN bus stays in recessive state and RxD_buskeeper is kept high.

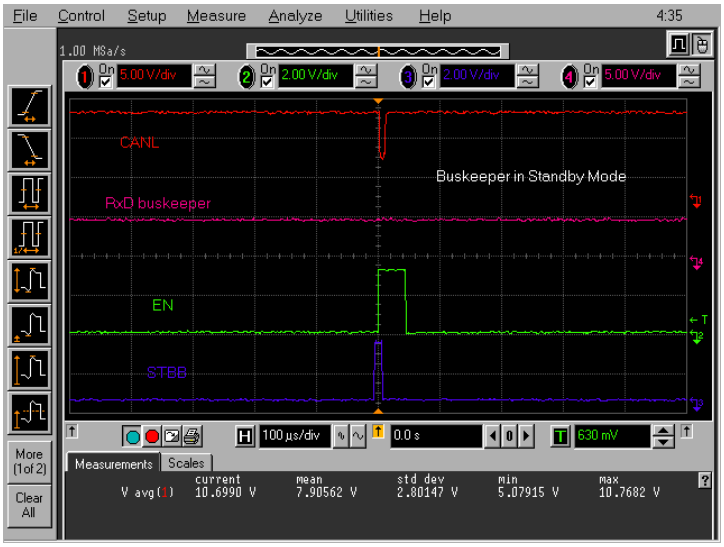


Figure 22. Buskeeper in normal mode. CANL termination switched to Vcc. No influence seen on CANL and on RxD_buskeeper.

Figures 23 and 24 are showing the influence on both CANL as CANH in a zoomed in and zoomed out time−scale. As can be seen the short change in CANL termination is hardly detectable on the oscilloscope (only in glitch mode), and for long time−base settings it can't be even observed.

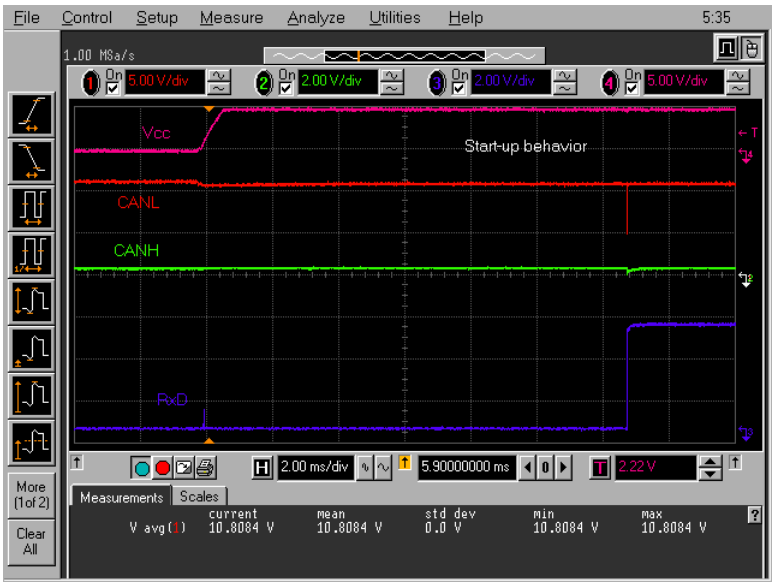


Figure 23. CANL termination switched from Vbat to Vcc for a short while (1.2 Tbit). No influence seen CANH. RxD switches high after the POR time−out.

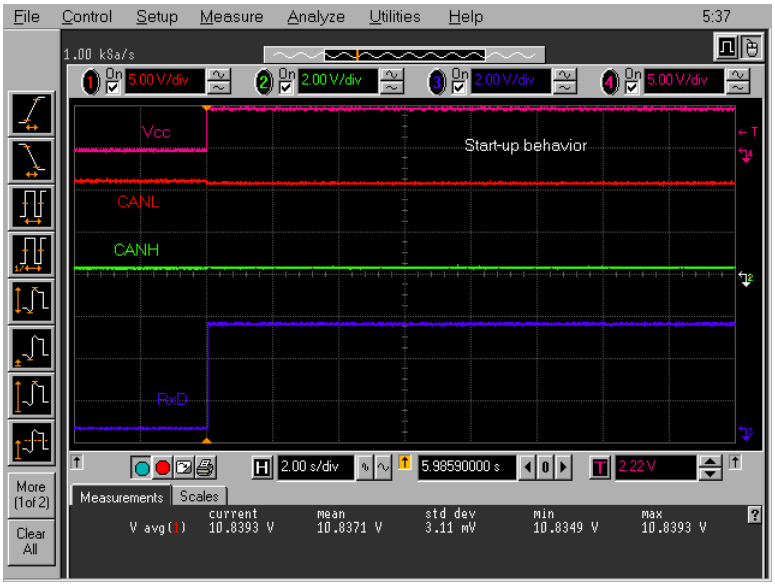


Figure 24. The CANL termination switched from Vbat to Vcc is not observable on a bigger time scale.

Conclusion

Under very specific conditions of power−on rise time and delay between Vbat and Vcc, it is possible that RxD stays 0 after start−up.

To guarantee that always RxD = 1 after start−up, it is advised to run a short sequence using the digital input pins STBB and EN.

The side effect of this sequence is that the transceiver enters Normal Mode for a few micro−seconds. This results in a short change in termination of the CANL line from Vbat to Vcc. The duration of this change in termination is about 1.2 Tbit for a given baud−rate = 125 kbit/s.

There is no effect on communication because the CANL level always stays above the receiver dominant threshold.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative